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Patentanmeldung Nr. | Patent application No. | Demande de brevet n°

03103233.7

PRIORITY DOCUMENT
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R C van Dijk

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Bezeichnung der Erfindung/Title of the invention/Titre de l'invention:
(Falls die Bezeichnung der Erfindung nicht angegeben ist, siehe Beschreibung.
If no title is shown please refer to the description.
Si aucun titre n'est indiqué se referer à la description.)

Electronic device comprising an LDMOS transistor

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Electronic device comprising an LDMOS transistor

The invention relates to an electronic device comprising a transistor provided at a surface of a semiconductor substrate, the transistor having a source and a drain electrode that are mutually connected through a channel and a gate electrode for influencing an electron distribution in the channel and a shield present between the gate and the drain electrode, which drain electrode is provided with a drain extension extending in the substrate towards the channel, the drain having a contact, said drain contact and said gate being mutually separated through an extension area.

The invention further relates to a method of manufacturing thereof.

In base stations for personal communications systems (GSM, EDGE, W-CDMA), the RF power amplifiers are one of the key components. For these power amplifiers, RF LDMOS transistors are now the preferred choice of technology [1] because of its excellent high power capabilities, gain and linearity. To be able to meet the demands imposed by new communication standards, the performance of LDMOS transistors is subject to continuous improvements [2]. Especially for W-CDMA systems, the linearity demands are very stringent which can only be met by operating the amplifier sufficiently far in back-off. However, this means that the efficiency decreases to typically ≈30%, and becomes an issue. It is this trade-off between linearity and efficiency that nowadays receives much attention.

It is therefore an object of the present invention to provide an electronic device of the kind described in the opening paragraph with an improved linearity-efficiency trade-off.

This object is achieved in that the shield has a stepped structure in the extension area. The stepped structure combines the advantages of the improved field distribution with a better current capability and on-resistance. The step construction diminishes the pinch action of the shield near the channel giving an improved on-resistance.

At the same time, the breakdown voltage is unaltered, as is imposed by the lower part of the stepped shield structure at the side facing away from the gate electrode.

The object is also achieved in that the drain extension is provided with a first and a second region, the first region having interfaces with the channel and the second region, the second region having an interface with a contact area within the drain electrode, wherein the first region has a higher dopant concentration than the second region, and the first region is substantially present within a shield area defined by a perpendicular projection of the shield on the substrate.

In a very suitable embodiment, both measures are combined to provide optimal performance. The combination leads to a total efficiency improvement at linear operation of about 6%.

The measures are particularly suitable for use in so-called LDMOS-transistors on the basis of a silicon substrate. However, they are suitable for other technologies as well. The result is a transistor that can be suitable used for a broad range of frequencies in the RF field, for instance from 800 MHz to 2,4 GHz. It is particularly suitable for use in a power amplifier.

Furthermore, the invention can be implemented in transistors with different channel length and different sizes of the extension area. These are parameters that are suitable for optimization of the device. In a suitable embodiment, use is made of an additional capacitor that can be driven by a separate contact (providing a four-terminal device). In another suitable embodiment, the transistor is provided as an array of parallelelly switched transistor segments, each of the segments having a first and a second threshold voltage. These embodiments are per se known from the non-prepublished applications EP03101224.8 (PHNL030460) and EP03101096.0 (PHNL030398), which are included by reference.

These and other aspects of the device of the invention will be further elucidated with reference to the Figures, that are not drawn to scale and purely diagrammatical, in which:

Fig. 1 shows a diagrammatical cross-sectional view of a prior art LDMOS device;

Fig. 2 shows a diagrammatical cross-sectional view of the device of the invention, including both high doping zone and stepped shield;

Fig. 3 shows the IMD3 performance of the device provided with a shield in a conventional and a stepped shape;

Fig. 4 shows the IMD3 performance versus the efficiency for the device with a shield in a conventional and a stepped shape;

Fig. 5 shows doping profiles along the surface of a uniform drain extension, a prior art device as shown in Fig. 1 and the device of the invention as depicted in Fig. 2;

Fig. 6 shows the electric field distribution at 26V along the surface in the drain extension region for the doping profiles of Fig. 5;

Fig. 7 shows the on-resistance Ron and the current capacity Idsx for the different shield construction and the different drain extension constructions;

Fig. 8 shows the IMD3 performance of the device provided with a uniform drain extension, with an LDD and with a HDD;

Fig. 9 shows the IMD3 versus the efficiency of the device with uniform drain extension, with an LDD and with a HDD; and

Fig. 10 shows the feedback capacitance Cgd for the device with uniform drain extension, with an LDD and with an HDD.

Fig. 1 depicts a cross-section of state of the art LDMOST technology. It consists of a silicided poly-silicon gate, a laterally diffused p-well, a p-sinker to connect the source to the highly doped substrate and a lowly doped drain extension region to accommodate high voltage operation. The source and drain electrode are each provided with a metallic contact. Between the gate and the channel an oxide layer is present. The source and drain electrodes each comprise a contact area that is highly doped (N+). The drain is provided with a drain extension extending towards the channel. The extension area is found between the gate electrode and the drain contact.

If the drain extension is uniformly doped and optimized for maximum output power hot carrier degradation will occur which manifests itself by a drift in the quiescent current (Idq) at constant Vgs. A step-wise doping profile, i.e. a first and a second lowly doped regions in the drain-extension (LDD1 and LDD2) [3], solves this problem at the cost of some RF-performance. The introduction of the dummy gate as shield [2], gives a better trade-off between Idq-degradation and RF-performance. The shield is connected to the source (in the 3rd dimension, not shown in Fig. 1) and acts as a field plate near the gate. Due to the close proximity of the shield to the gate and drain extension, the electric field distribution in

the drain extension improves reducing both degradation and feedback capacitance. Another trade-off now becomes dominant: That between breakdown voltage (BV) versus current capability (Idsx) and on-resistance (Ron).

Fig. 2 shows a diagrammatical cross-sectional view of the device of the invention. Herein, two major improvements to the prior art have been made. The improvements contribute both to the optimal performance and are preferably applied in combination. However, it is not excluded that the two improvements are applied separately. This is particularly the case in view of the fact that the present examples relate to transistors suitable for use in basestations. These are designed so as to have a very high breakdown voltage, and a high power and voltage. The same improvements can be applied for instance power amplifiers in mobile phone applications. The requirements regarding linearity and efficiency are therein the same, but the breakdown voltage is lower, whereas the power consumption is very critical. The design can be optimized for the specific application, for instance by varying the doping concentration in the drain extension. For basestations, such concentration is in the order of 10^{12}, whereas for mobile phones the concentration is generally higher.

The first improvement is the stepped shield structure. The stepped structure is provided in an extension area present between the gate and the drain contact. Preferably, the stepped structure is present in the vicinity of the gate electrode. This structure combines the advantages of the improved field distribution with a better current capability and on-resistance Ron. The step construction diminishes the pinching action of the shield near the channel giving an improved Ron and an improved current capability Idsx (Fig. 7). At the same time, the breakdown voltage is unaltered as imposed by the lower part of the shield on the right hand side. The present Figures show an example of a device made in the LDMOS technology in a silicon substrate. It is however not excluded that use is made of alternative semiconductor substrates, such as SiGe or even a III-V material substrate, such as GaAs.

As can be seen in Fig. 2, the stepped shield is provided in an advantageous manner by deposition of the shield layer on top of an L-spacer. The provision of such an L-spacer is known per se from WO-A 02/049092, that is included herein by reference. The gate of the present device is made of polysilicon. However, a metal gate may be used alternatively. The stepped shield structure as shown can be subdivided in two sections: an inversed L-shaped section and a z-shaped section. It is the insight that the z-shaped section is essential for the performance of the device, so as to minimize the parasitic capacity between the source and the gate, while maintaining or improving the efficiency, at the same or similar

breakdown voltage. The inversed L-shaped section is present as a consequence of the technology used during the experiments leading to the invention. However, in a further technological development, particularly by using photoresists that allow higher resolutions, the inversed L-shaped section can be reduced in size, or even be completely absent. This would be advantageous for the reduction of the parasitic capacitance. In a further embodiment, the stepped shield structure is provided with an extension substantially transversal to the substrate surface. Such an extension is considered to have a beneficial influence on the shielding function.

Figs. 3 and 4 show the two-tone large signal RF-performance of a device having a channel length of 18 nm. The linearity is of primary importance for the RF performance, and this linearity is generally measured as the higher (uneven) order intermodulation distortion. Particularly the third order intermodulation distortion is critical. This distortion will also be referred to as IMD3. Further explanation regarding the IMD3 is described in the pending patent applications EP03101224.8 (PHNL030460) and EP03101096.0 (PHNL030398), which are included by reference. At linear operation, at -40dBc IMD3, both the output power increases and the linearity-efficiency trade-off improves for the stepped shield. The stepped construction of the shield has been fabricated in a 0.6 μm gate length process using nitride L-spacers next to the gate. On top of the oxide/nitride stack the shield is formed by depositing either a low resistive metal or silicided poly-silicon layer. The low resistance of the shield leads away the RF current imposed on the shield by the gate and drain, resulting in an RF shielding action. The stepped structure has the big advantage that a stepped profile as used in the prior art is no longer needed to keep hot carrier degradation in control. The extension can thus be doped as is desired or preferred, hence uniform, stepped with low dopant profiles or with higher dopant profiles.

The second major improvement of the invention resides in the use of a heavily doped drain region in combination with a low doped drain region. The heavily doped region is the first region. This heavily doped drain region will also be referred to as HDD. The low doped drain region is the second region, and will also be referred to as LDD. The notion ' heavy' must be regarded in comparison to 'low'. Preferably, the ratio between heavy and low is between 1,2 and 3, by further preference between 1,3 and 2,5 and most preferred in the range of 1,5 and 2. The higher limitation is due in order to realize a sufficient breakdown voltage. For some applications, this is less critical. The use of a high and low doped drain region is preferably combined with the measure that the HDD extends laterally within the area covered by the shield. However, the use of a HDD next to a LDD turns out to have a

beneficial effect even if no shield would be present at all – which is however unlikely for RF applications. Preferably, the HDD is even somewhat smaller than the area covered by the shield.

To examine the effect of LDD or HDD, devices were processed with three different doping profiles: an uniform drain extension, an LDD and HDD profile (Fig. 5). Usually a higher dope means also a lower breakdown voltage. When, however, the HDD region is restricted to the area below the shield, the peak electric field in the remaining drain extension does not change, see Fig. 6, and the BV remains unaltered. The higher dope concentration has, however, a large impact on Ron and current capacity Idsx (Fig. 7). Both improve significantly with the use of an HDD. Figs. 8 and 9 show the two-tone large signal RF-performance. At linear operation, at around -40dBc IMD3, the output power again increases and also the linearity-efficiency trade-off improves with HDD. With the higher dope the feedback capacitance increases but this is limited to lower voltage (Fig. 10).

REFERENCES:

A. Wood, C. Dragon and W Burger, "High performance Si LDMOS technology for 2GHz RF power amplifier applications", IEDM tech. Dig., pp. 87-90, 1996.

S. Xu, F. Baiocchi, H. Safar, J. Lott, A. Shibib, Z. Xie, "High Power Silicon RF LDMOSFET Technology for 2.1 GHz Power Amplifier Applications.", IEEE ISPSD, pp, 2003.

S. Xu, P. Foo, J. Wen, Y. Liu, F. Lin and C. Ren, "RF LDMOS with Extreme Low Parasitic Feedback Capacitance and High Hot-Carrier Immunity", IEDM tech. Dig., pp, 1999.

CLAIMS:

1. An electronic device comprising a transistor provided at a surface of a semiconductor substrate, the transistor having a source and a drain electrode that are mutually connected through a channel and a gate electrode for influencing an electron distribution in the channel and a shield present between the gate and the drain electrode, which drain electrode is provided with a drain extension extending in the substrate towards the channel, the drain having a contact, said drain contact and said gate being mutually separated through an extension area, characterized in that the shield has a stepped structure in the extension area.

2. An electronic device as claimed in claim 1, wherein a L-shaped spacer is present between the gate-electrode and the shield.

3. An electronic device as claimed in claim 1 or 2, wherein the shield is formed as a metal silicide.

4. An electronic device as claimed in claim 1 or 2, wherein the drain extension is provided with a first and a second region, the first region having interfaces with the channel and the second region, the second region having an interface with a contact area within the drain electrode, which first region has a higher dopant concentration than the second region, and wherein the first region is substantially present within a shield area defined by a perpendicular projection of the shield on the substrate.

5. An electronic device comprising a transistor provided at a surface of a semiconductor substrate, the transistor having a source and a drain electrode that are mutually connected through a channel and a gate electrode for influencing an electron distribution in the channel and a shield present between the gate and the drain electrode, which drain electrode is provided with a drain extension extending in the substrate towards the channel, the drain having a contact, said drain contact and said gate being mutually separated through an extension area, which drain extension is provided with a first and a second region, the first

region having interfaces with the channel and the second region, the second region having an interface with a contact area within the drain electrode wherein the first region has a higher dopant concentration than the second region, and the first region is substantially present within a shield area defined by a perpendicular projection of the shield on the substrate.

6. An electronic device as claimed in claim 4 or 5, wherein the interface between the first and the second region is present within the shield area.

7. An electronic device as claimed in claim 4, 5 or 6, wherein the ratio of the dopant concentrations in the first and the second region is in the range of 1.2 to 2.5.

8. An electronic device as claimed in claim 1 or 5, wherein the shield is electrically connected to the source electrode through an electrical connection.

9. An electronic device as claimed in claim 9, wherein the electrical connection comprises a capacitor.

10. An electronic device as claimed in claim 1 or 5, wherein the semiconductor substrate is made of silicon and the transistor is of the LDMOS type.

11. A method of manufacturing an electronic device as claimed in claim 2, comprising the steps of:

- providing a transistor including source, drain and gate electrode as well as drain extension;
- providing an L-shaped spacer neighboring the gate electrode; and
- providing a stepped shield structure by metal deposition on the L-shaped spacer.

ABSTRACT:

The LDMOS transistor of the invention is provided with a stepped shield structure and/or with a first and a second drain extension region, the first drain extension region having a higher dopant concentration than the second drain extension region, and being covered by the shield.

Fig. 2

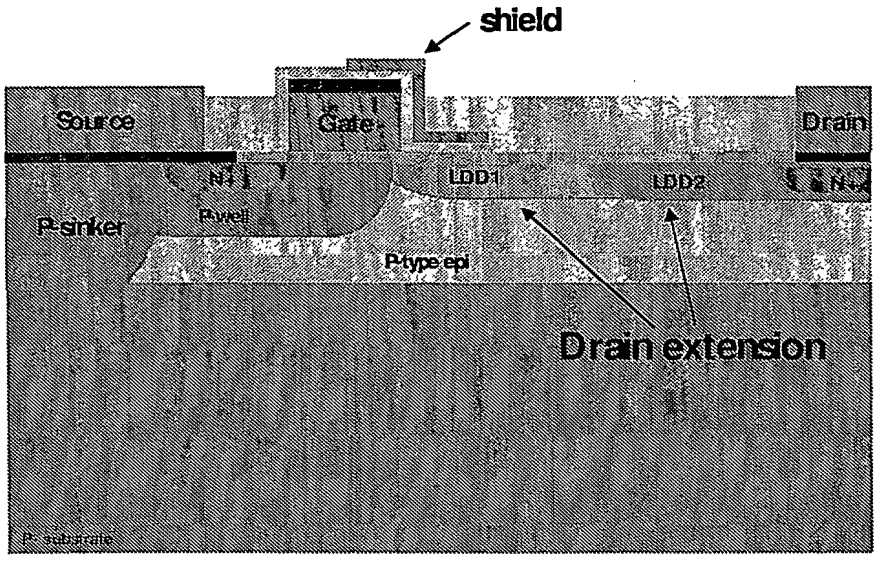
shield
Source
Gate
Drain
N+
LDD1
LDD2
N+
P-sinker
P-well
P-type epi
Drain extension

FIG.1

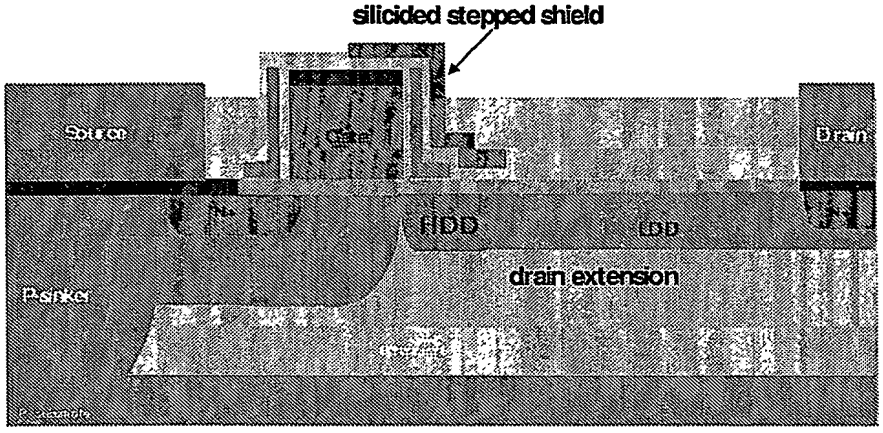
silicided stepped shield
Source
Gate
Drain
N+
HDD
LDD
drain extension
P-sinker

FIG.2

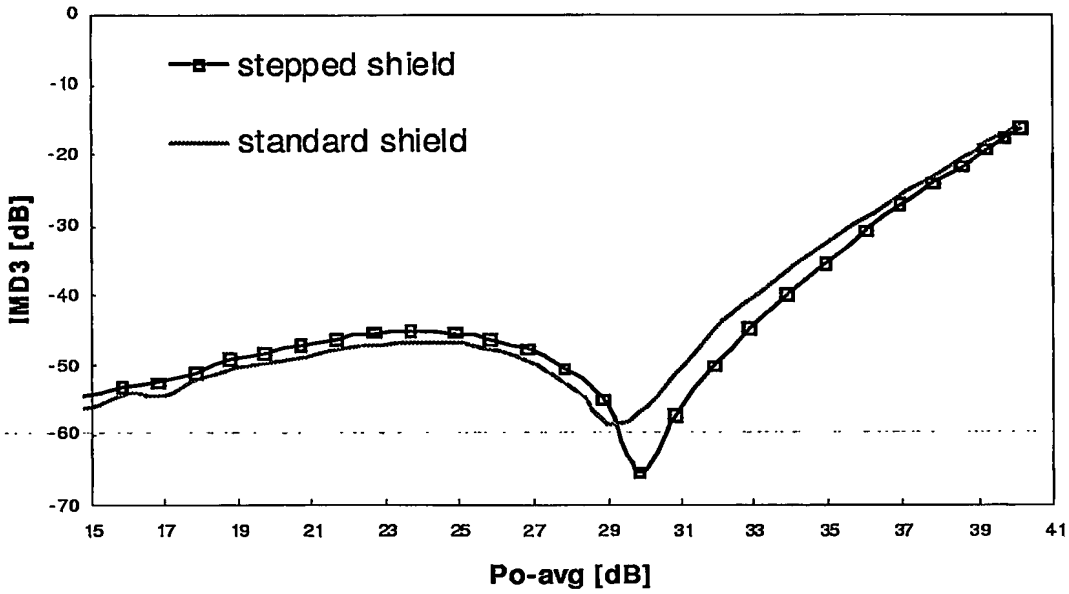
stepped shield
standard shield
IMD3 [dB]
0
-10
-20
-30
-40
-50
-60
-70
15
17
19
21
23
25
27
29
31
33
35
37
39
41
Po-avg [dB]

FIG.3

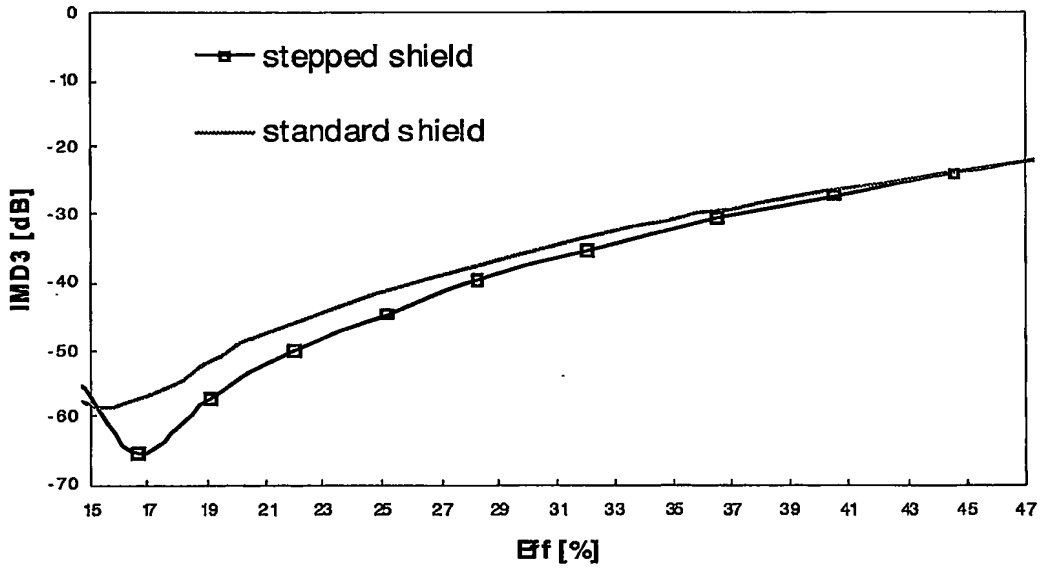
stepped shield
standard shield
IMD3 [dB]
0
-10
-20
-30
-40
-50
-60
-70
15
17
19
21
23
25
27
29
31
33
35
37
39
41
43
45
47
Eff [%]

FIG.4

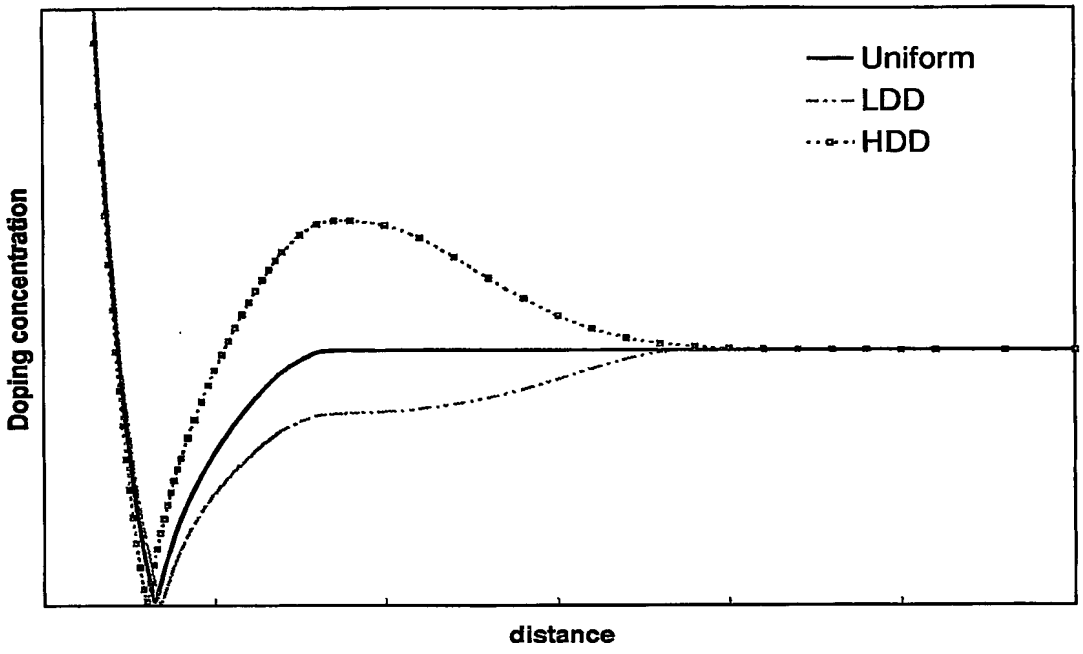
Uniform
LDD
HDD
Doping concentration
distance

FIG.5

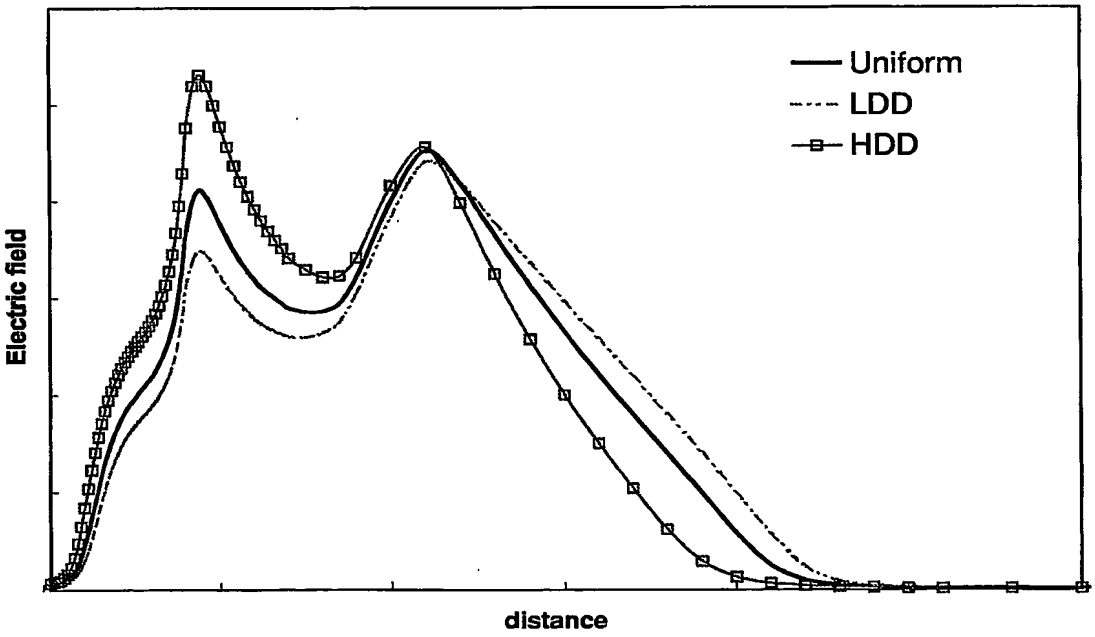
Uniform
LDD
HDD
Electric field
distance

FIG.6

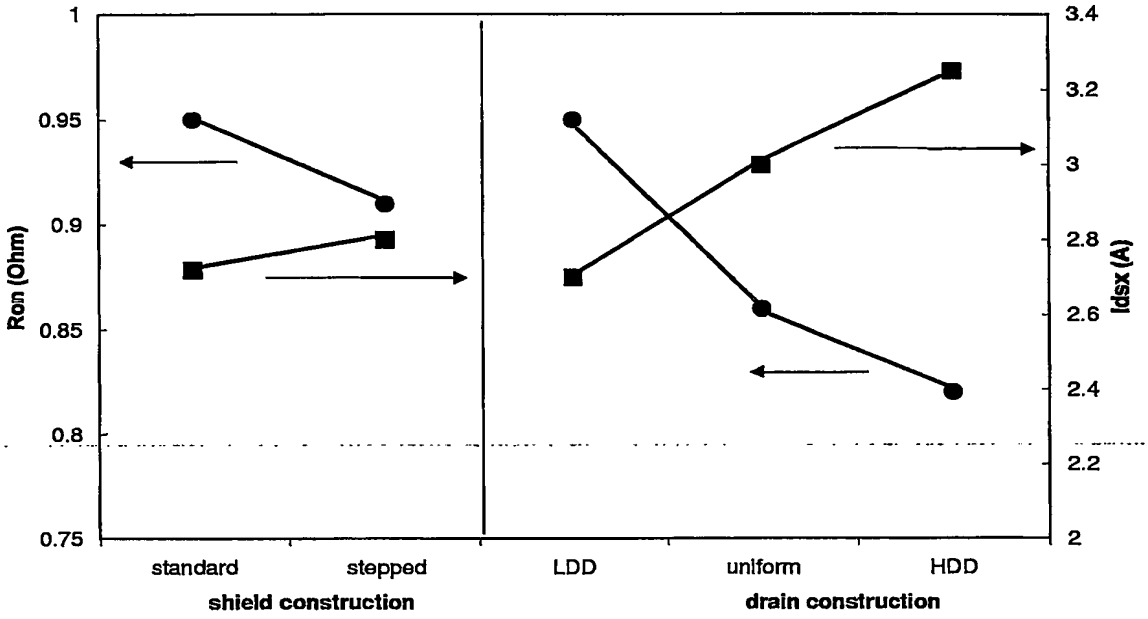
1
0.95
0.9
0.85
0.8
0.75
Ron (Ohm)
3.4
3.2
3
2.8
2.6
2.4
2.2
2
Idsx (A)
standard
stepped
LDD
uniform
HDD
shield construction
drain construction

FIG.7

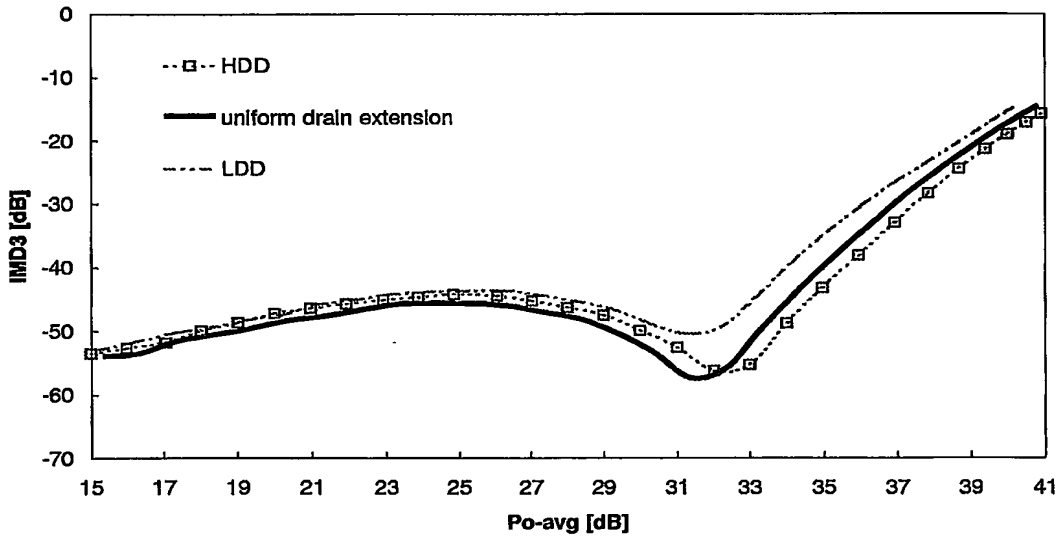
0
-10
-20
-30
-40
-50
-60
-70
IMD3 [dB]
HDD
uniform drain extension
LDD
15
17
19
21
23
25
27
29
31
33
35
37
39
41
Po-avg [dB]

FIG.8

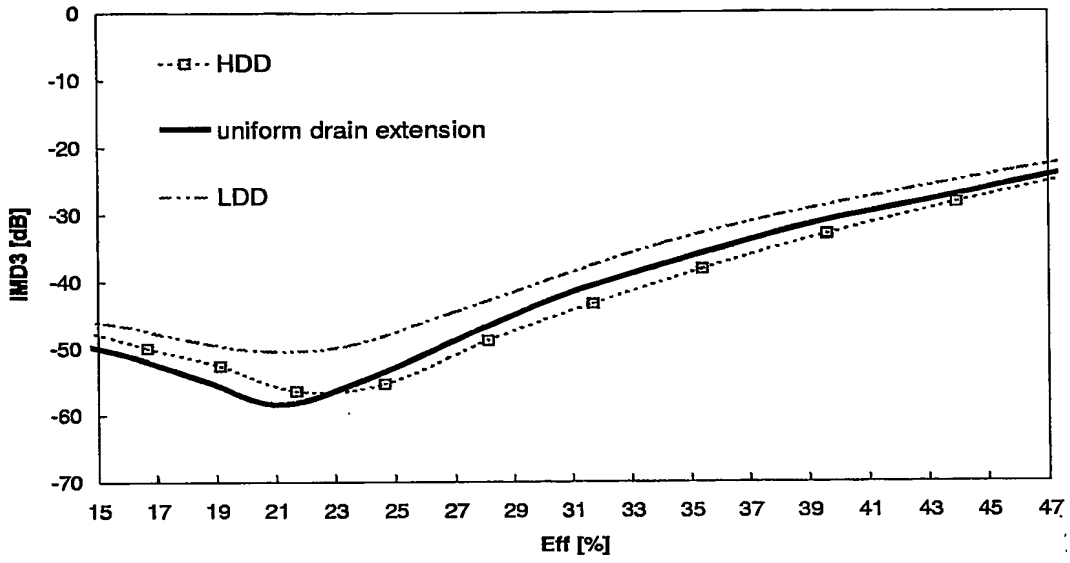
HDD
uniform drain extension
LDD
IMD3 [dB]
Eff [%]
0
-10
-20
-30
-40
-50
-60
-70
15
17
19
21
23
25
27
29
31
33
35
37
39
41
43
45
47

FIG.9

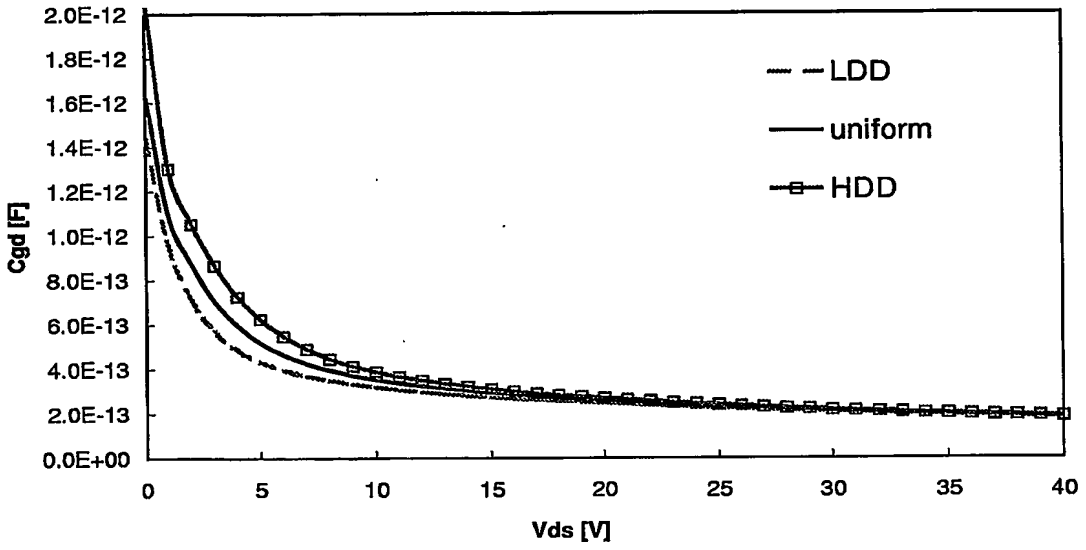
LDD
uniform
HDD
Cgd [F]
Vds [V]
2.0E-12
1.8E-12
1.6E-12
1.4E-12
1.2E-12
1.0E-12
8.0E-13
6.0E-13
4.0E-13
2.0E-13
0.0E+00
0
5
10
15
20
25
30
35
40

FIG.10